

DERWENT-ACC-NO: 2004-287378

DERWENT-WEEK: 200427

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TITLE: Semiconductor memory e.g. metal oxide nitride oxide semiconductor memory has one pair of insulating layers with nitridation films, that are formed so that control gates and another pair of layers formed on gates, are covered

PATENT-ASSIGNEE: SEIKO EPSON CORP[SHIH]

PRIORITY-DATA: 2002JP-0223708 (July 31, 2002)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 2004064012 A	February 26, 2004	N/A	022	H01L 021/8247

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP2004064012A	N/A	2002JP-0223708	July 31, 2002

INT-CL (IPC): H01L021/8234, H01L021/8247, H01L027/088, H01L027/10, H01L027/115, H01L029/788, H01L029/792

ABSTRACTED-PUB-NO: JP2004064012A

BASIC-ABSTRACT:

NOVELTY - The control gates (20,30) are formed at both sides of a word gate (14) formed on a substrate (10) through oxide nitride-oxide (ONO) films. One pair of sidewall insulating layers (52) is formed at upper portions of the control gates. Another pair of sidewall insulating layers (54) with nitridation films, is formed at the sides of the gates so that the control gates and the insulating layers (52) are covered.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing method of semiconductor memory.

USE - Semiconductor memory e.g. metal oxide nitride oxide semiconductor (MONOS) memory and silicon oxide nitride oxide semiconductor (SONOS) memory.

ADVANTAGE - Prevents exposure of natural oxidation film, before silicide formation, by forming sidewall insulating layer with nitridation film.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the semiconductor memory.

semiconductor substrate 10

gate insulating layer 12

word gate 14

impurity layers 16,18

control gates 20,30

sidewall insulating layers 50,52,54

memory cell 100

metal oxide semiconductor transistor 500

memory range 1000

logic circuit range 2000

CHOSEN-DRAWING: Dwg.3/19

TITLE-TERMS: SEMICONDUCTOR MEMORY METAL OXIDE NITRIDE OXIDE SEMICONDUCTOR

MEMORY ONE PAIR INSULATE LAYER NITRIDATION FILM FORMING SO CONTROL

GATE PAIR LAYER FORMING GATE COVER

DERWENT-CLASS: L03 U11 U14

CPI-CODES: L04-C11C1; L04-C12A; L04-C12B;

EPI-CODES: U11-C05B5; U11-C05F1; U14-A03B7;

SECONDARY-ACC-NO:

CPI Secondary Accession Numbers: C2004-110861

Non-CPI Secondary Accession Numbers: N2004-227951

80 配線層

100 不揮発性記憶装置（メモリセル）

120 絶縁層

122 第3ゲート絶縁層

140, 140a, 140b ゲート層

142 ゲート電極

160, 180 開口部

162, 182 不純物層

270 絶縁層

300 素子分離領域

10

400 コンタクト用不純物層

500 絶縁ゲート電界効果トランジスタ（MOSトランジスタ）

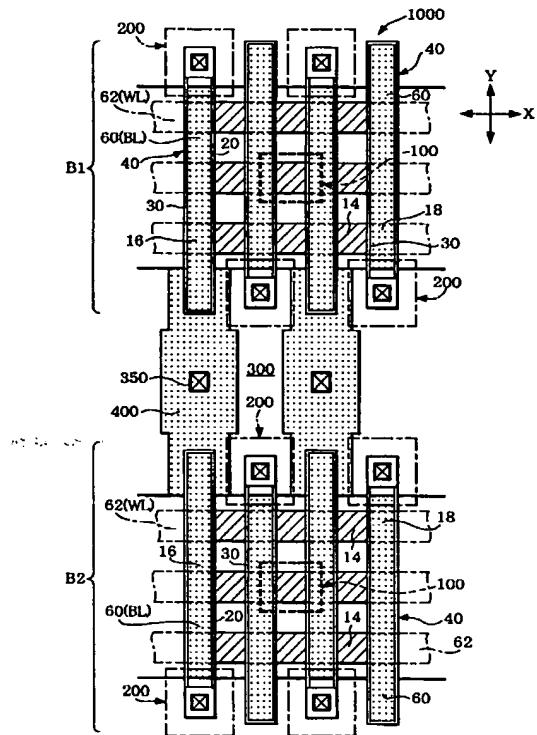
S100 ストップ層

R100, R200, R300 レジスト層

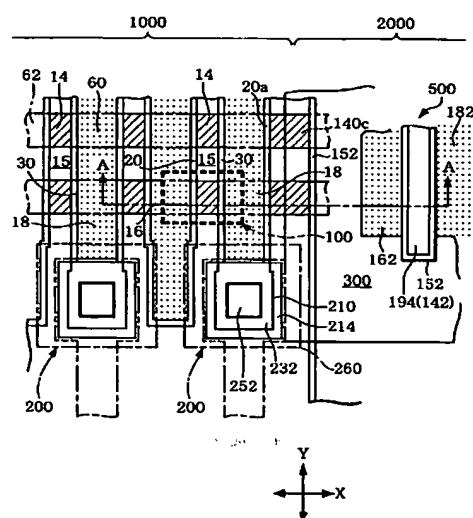
1000 メモリ領域

2000 ロジック回路領域

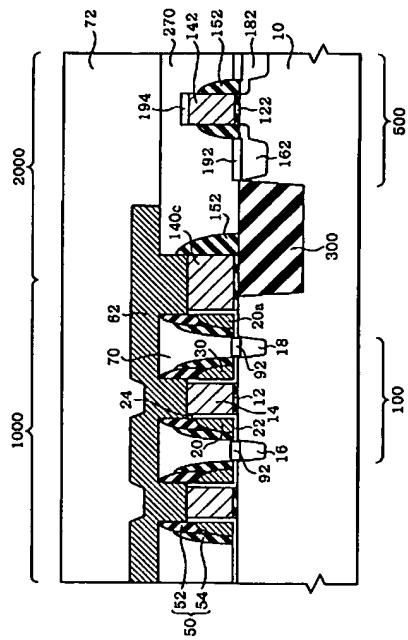
【図1】



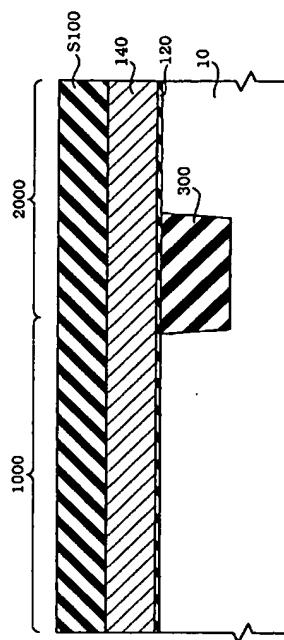
【図2】



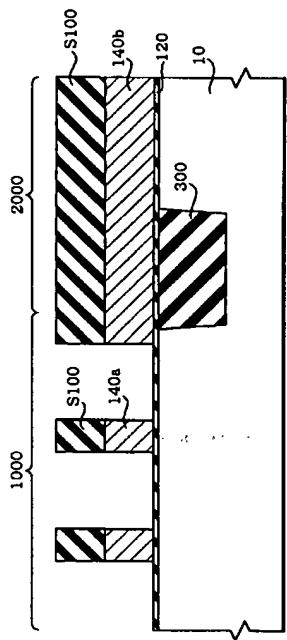
【図3】



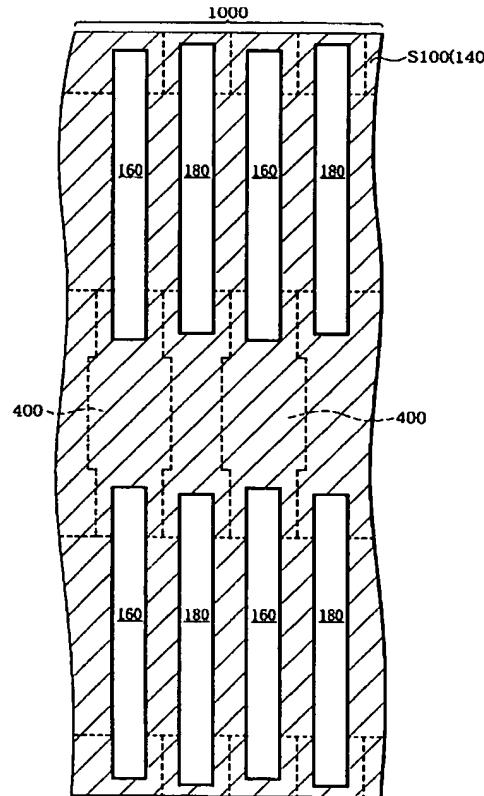
【图4】



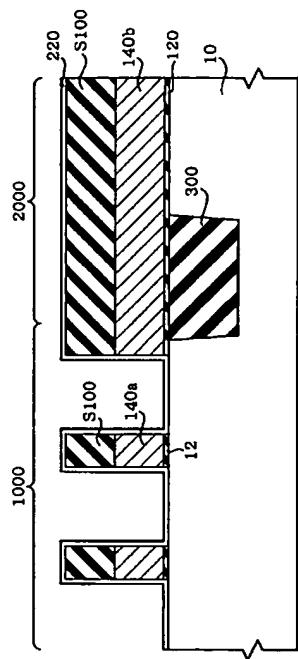
【圖 5】



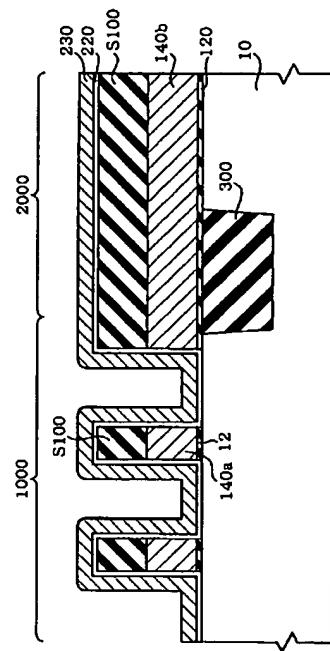
【图 6】



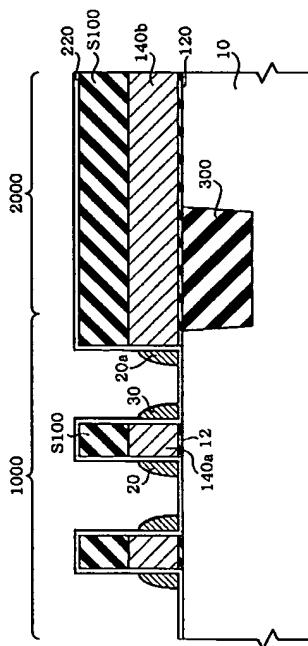
【図 7】



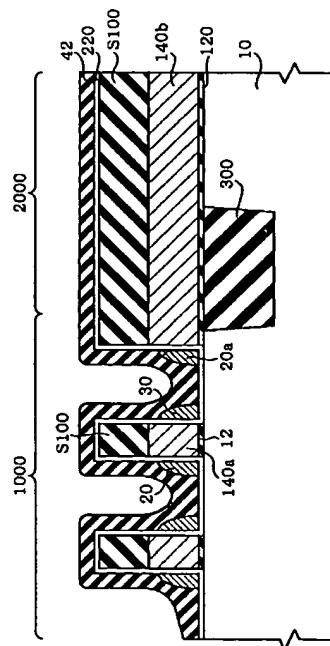
【図 8】



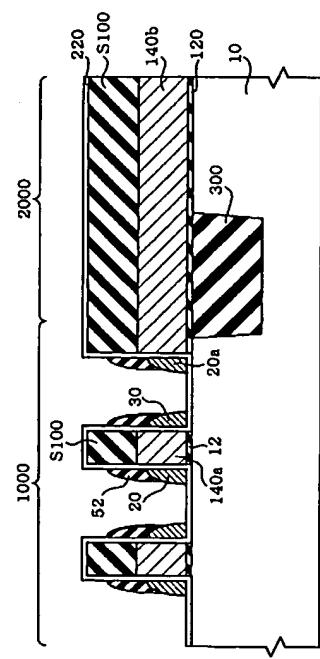
【図 9】



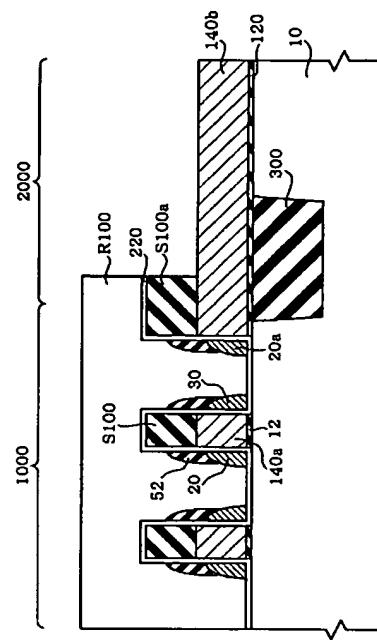
【図 10】



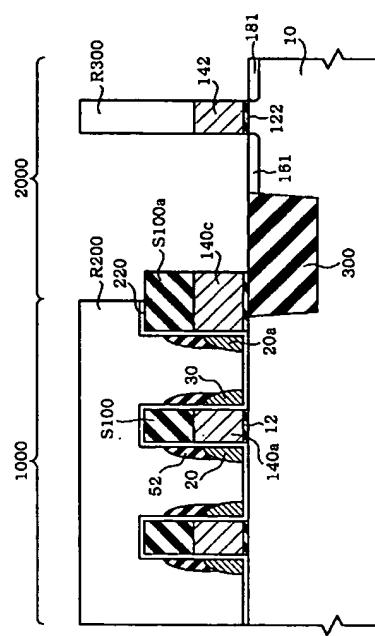
【図 1 1】



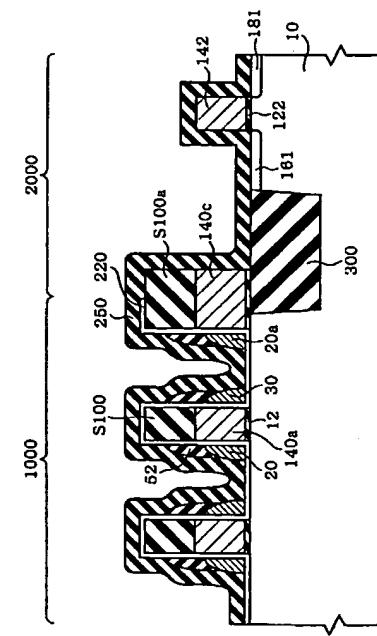
【図 1 2】



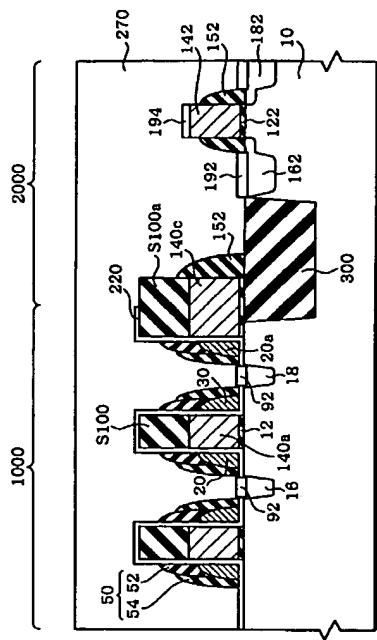
【図 1 3】



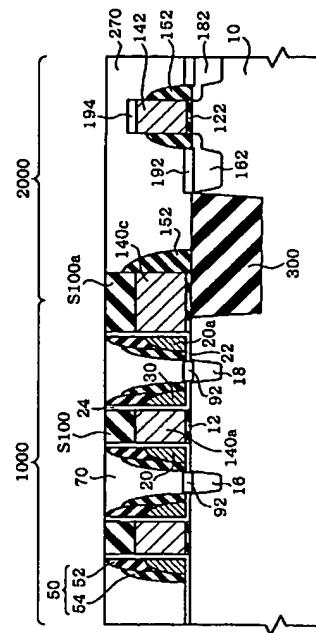
【図 1 4】



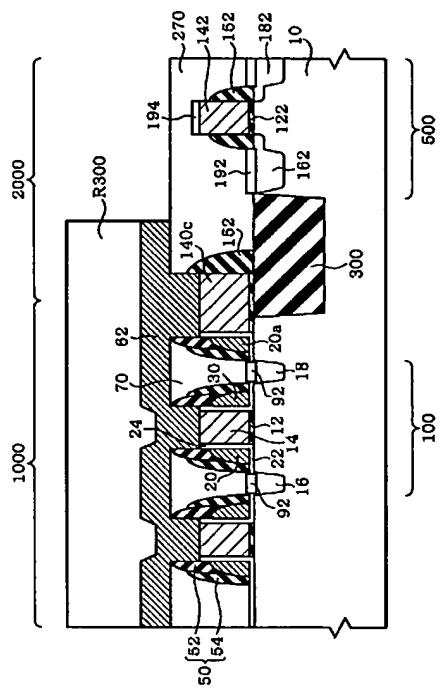
【図15】



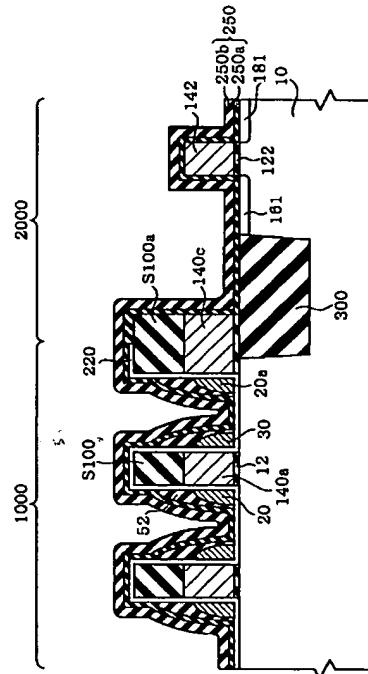
【四 1 6】



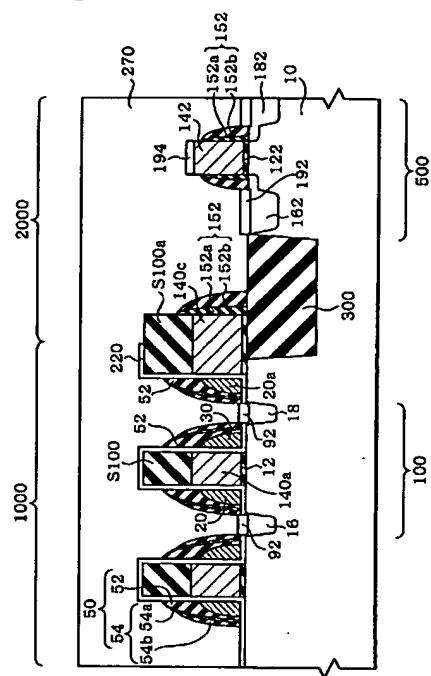
【図 17】



【図18】



【図 19】



【図 20】

